IN THE SPECIFICATION:

Please amend the first full paragraph appearing on page 1, including the section title immediately preceding it, as was inserted by the Preliminary Amendment dated November 27, 2000, as follows:

Cross-Reference to Related Application

This application is a divisional of application serial no. 08/773,272, filed December 23, 1996, now ~~pending.~~ U.S. Patent 6,153,358, issued November 28, 2000.

Please amend the eleventh full paragraph appearing on page 2 as follows:

Fig. 9A shows a ~~cross-sectional~~ cross-sectional view of a portion of a field emission device (FED) during an intermediate state of the fabrication of the FED;

Please amend the twelfth full paragraph appearing on page 2 as follows:

Fig. 9B shows a ~~cross-sectional~~ cross-sectional view of the FED of Fig. 9A following planarization;

Please amend the paragraph bridging pages 2 and 3 as follows:

Fig. 9C shows a ~~cross-sectional~~ cross-sectional view of the FED of Fig. 9B following vapor HF etching according to the invention;

Please amend the first full paragraph appearing on page 3 as follows:

Fig. 9D shows a ~~cross-sectional~~ cross-sectional view of a FED prior to vapor HF etching and including a patterned polyimide layer; and

Please amend the second full paragraph appearing on page 3 as follows:

Fig. 9E shows a ~~cross-sectional~~ cross-sectional view of a FED prior to vapor HF etching and including passivation and patterned polyimide layers.

Please amend the third full paragraph appearing on page 3 as follows:

Fig. 1 is a flow chart illustrating steps of an etching process carried out pursuant to the principles of the invention. Individually, each step is carried out through the use of conventional process techniques and materials well known to those having ordinary skill in the art. This process may be performed on any material capable of being etched (i.e., "etchable material") such as silicon dioxide. Fig. 2A, for example, shows etchable material in the form pf a silicon dioxide layer 204 which is formed over a silicon substrate 202. These layers combine to form ~~assembly~~ structure 250. Substrate 202 may be a single crystal silicon layer. Alternatively, substrate 202 may be constructed from one or more semiconductor layers or structures that include active or operable portions of semiconductor devices. In the following description, ~~assemblies 250-262~~ structures 250, 252, 254, 256, 258, 260 and 262 (Figs. 2A-2G) will be used to illustrate the process of Fig. 1.

Please amend the paragraph bridging pages 3 and 4 as follows:

Referring to block 102 of Fig. 1, initially, structure 250 is cleaned in preparation for the forming of a polyimide layer. Such cleaning enhances the adhesiveness of polyimide to the underlying layer. This step may be carried out through the use of a variety of conventional materials including: ~~ST-22~~ ST-22™ (positive photoresist stripper) available from Advanced ~~Chemical Systems International,~~ Technology Materials, Inc., having a principal place of business at ~~1200 West Jackson Road, Carrollton, Texas ("ACSI");~~ 7 Commerce Drive, Danbury, Connecticut ("ATMI"); Photoresist Stripper Rinse ("PSR") also available from ~~ACSI;~~ ATMI; and deionized water. Structure 250 is initially immersed in ST-22 for approximately 15 minutes at about 85°C. The structure 250 is next immersed in PSR for approximately 10 minutes at about 25°C i.e., room temperature). Finally, structure 250 is immersed in deionized water for approximately 5-10 minutes, again at room temperature.

Please amend the first full paragraph appearing on page 4 as follows:

Referring to blocks 104 and 106 in Fig. 1, layers of polyimide and photoresist are next deposited on the etchable material (i.e., silicon dioxide layer 204). These steps are illustrated by structure 252 of Fig. 2B, which shows photoresist layer 208 disposed on top of polyimide layer 206 which is, in turn, disposed on top of silicon dioxide layer 204. ~~Layer~~ Polyimide layer 206 may be deposited using standard photoresist spin coating techniques. As is well known, layer thickness is dependent upon spin speed. For example, spin speeds of about 5000 rpm and 2300 rpm produce polyimide layers of about 5.4 micrometers and 11.7 micrometers thick, respectively. (The allowable duration of vapor HF etching is dependent at least in part upon the thickness of polyimide layer 206.) After depositing the polyimide layer 206, the resulting structure is baked for approximately 120 seconds at about 130°C to remove solvents from the top of the structure. Any commercially available polyimide may be used, such as du Pont PI-1111 available from E.I. du Pont de Nemours and Company, headquartered at 1007 Market Street, Wilmington, Delaware 19898.

Please amend the second full paragraph appearing on page 4 as follows:

Referring again to Fig. 1, a positive photoresist layer is next deposited over the polyimide layer pursuant to block 106. Referring to Fig. 2B, photoresist layer 208 is also deposited using standard photoresist spin coating techniques. Preferably, photoresist layer 208 is deposited at a spin speed of approximately 3000 rpm to achieve, a thickness of approximately 1.45 micrometers. After depositing this material, structure 252 is baked for approximately 60 seconds at about 90°C. Any commercially available photoresist may be used, such as OiR 897-10i (positive photoresist) available from OCG Microelectronics Materials, Inc., located at Three Garret Mountain Plaza, West Paterson, New Jersey 07424.

Please amend the paragraph bridging pages 4 and 5 as follows:

After deposition, photoresist layer 208 is exposed through a standard lithographical mask, pursuant to block 108 in Fig. 1. Such exposure alters the molecular structure of photoresist

layer 208 in selected areas pursuant to a pattern defined by the lithographical mask. This step is illustrated in Fig. 2C, which shows a portion of a lithographical mask 210 disposed above photoresist layer 208.

Please amend the first full paragraph appearing on page 5 as follows:

As is well known in the art, mask 210 selectively controls exposure of the underlying photosensitive surface to ionizing radiation 212 (e.g., ultraviolet light or low energy x-rays). A portion of radiation 212 is stopped by mask 210 while the remainder is allowed to pass through the mask 210 and alter the underlying material pursuant to the pattern of the mask 210. In this case, radiation 212 is allowed to expose positive photoresist layer 208 at area 214. The preferred radiation exposure dose is approximately 250 mj of ultraviolet light.

Please amend the second full paragraph appearing on page 5 as follows:

After exposure, photoresist layer 208 is developed and underlying portions of polyimide layer 206 are removed by a multi-step operation pursuant to block 110 of Fig. 1. Initially, structure 254 (Fig. 2C) is baked at approximately 120°C for about 60 seconds. Next, ~~this~~ structure 254 is exposed to a solvent such as HPRD 435 (available from the Olin Corporation, which is located at 501 Merritt 7, Norwalk, Connecticut 06856) using a commercially available developer, such as the Developer Trek (available from Silicon Valley Group, Inc., which is located at 101 Metro Drive, San Jose, California 95110). Specifically, structure 254 is spun by the developer in conventional fashion while the surface is alternatingly sprayed with.HPRD 435 and deionized water in accordance with the sequence set out in Table 1.

Please amend the first full paragraph appearing on page 6 as follows:

The net result of ~~developing step~~ block 110, as seen in FIG. 1, is to develop photoresist and remove exposed portions of photoresist layer 208 and any underlying polyimide layer 206 uncovered from the removal of such exposed portions of photoresist layer 208. This process produces structure 256 of Fig. 2D. As shown in ~~this figure, a portion of layers~~ FIG. 2D, portions

of photoresist layer 208 and polyimide layer 206 have been removed leaving a gap 215. Accordingly, photoresist layer 208 is patterned in accordance with mask 210, and polyimide layer 206 is patterned in accordance with photoresist layer 208.

Please amend the second full paragraph appearing on page 6 as follows:

Referring again to Fig. 1, the next step in this process is to strip the photoresist layer 208 from the underlying polyimide layer 206 pursuant to block 112. In this case, photoresist layer 208 is stripped through the use of any conventional plasma process well known to those having ordinary skill in the art. Plasma is necessary because polyimide layer 206 is not yet cured and therefore use of a solvent to strip the photoresist layer 208 would also dissolve some of the polyimide layer 206, which is undesirable. Stripping of the photoresist layer 208 results in structure 258 of Fig. 2E.

Please amend the paragraph bridging pages 6 and 7 as follows:

Polyimide layer 206 is cured before it is used as an etching mask 220. Accordingly, referring to Fig. 1, the next step in this process is to cure polyimide layer 206 pursuant to block 114. The curing step preferably uses a 3-cycle heating process. Initially, structure 258 (Fig. 2E) is heated to approximately 135°C for about 3 hours. The temperature is then increased to approximately 300°C and sustained for about another 2 hours. Finally, the temperature is returned to 135°C and sustained for about another 3 hours. This 3-cycle approach is preferred because it provides a gradual increase and decrease in temperature of the polyimide layer 206. If this polyimide layer 206 is heated too quickly, cracks may develop in the polyimide layer 206 because exterior portions will expand faster than interior portions. The thickness of polyimide layer 206 will undergo a slight reduction due to this curing step. Upon completion of these curing cycles, polyimide layer 206 now forms an etching mask 220 over silicon dioxide layer 204. ~~Mask~~ Etching mask 220, having a pattern derived from lithographical mask 210 (through photoresist layer 208), will facilitate vapor HF etching as described below. For clarity,

structure 258 is referred to herein as "cured structure 258" upon completion of the curing step of block 114.

Please amend the paragraph bridging pages 7 and 8 as follows:

The operations and parameters preferably used to etch silicon dioxide using vapor HF pursuant to block 116 in Fig. 1 are set out below in Table 2 (all numerical values in this table are approximate). The five operations identified in Table 2, each of which is performed at room temperature ~~(i.e.,~~ (i.e., about 25°C), are collectively referred to as the "vapor HF etching cycle." Referring to Table 2, "Excaliber Control" represents the percentage of total flow available of a particular gas in the Excaliber System. The corresponding flow rate in terms of SLM (Standard Liters Per Minute) and SCCM (Standard Cubic Centimeters Per Minute) is provided in the table. In each operation of the cycle, the "material" (i.e., gas) identified in Table 2 is passed across the surface of the subject structure (e.g., cured structure 258 of Fig. 2E) pursuant to the flow rate in the table. The ratio of N_2 gas to vapor H_2O in the "pretreat" etching operation is about 5 to 1. The ratio of N_2 gas to Vapor H_2O to HF vapor in the "etch" step is approximately 150 to 30 to 7. Given the combination of elements and flow rates as provided in Table 2, the resulting etch rate of this operation is approximately 1000 angstroms for every 10 seconds.

Please amend the paragraph bridging pages 8 and 9 as follows:

As shown in Table 2, the first operation of the etching cycle is an "initial purge" which removes oxygen (O_2) from the surface of cured structure 258 (Fig. 2E). This is carried out by exposing the surface of cured structure 258 to N_2 gas in accordance with the parameter set out in Table 2. Next, the surface of cured structure 258 undergoes a "pretreat" operation with N_2 gas and vapor H_2O in accordance with the parameters of Table 2. Pretreatment is followed by actual etching which, as noted above, uses the elements of N_2 gas, vapor H_2O and vapor HF. The speed of this "etch" operation is enhanced by adding H_2O to the vapor HF. As noted above, the etch rate for the operation shown in Table 2 is approximately 1000 angstroms per 10 seconds. Accordingly, a 20 second etch operation (the maximum duration indicated in Table 2) results in

an etch of approximately 2000 angstroms. (In contrast, eliminating vapor H_2O from this process reduces the etching rate to about 60 angstroms per 10 seconds.) Next, residual HF is removed through the "dilute HF" operation described in Table 2. Finally, a "high purge" operation is performed in accordance with the parameters set out in Table 2 to dry the surface of cured structure 258. These five operations may be repeated until a desired etch depth is achieved.

Please amend the first full paragraph appearing on page 9 as follows:

In accordance with the cycle of Table 2, etching may be carried out continuously for up to about 20 seconds. Continuous etching for a period longer than this time may cause ~~polyimide~~ etching mask 220 to crack. Should additional etching be desired, the five-step vapor HF etching cycle may be repeated as many times as necessary to achieve the desired depth, with the etch step in each cycle lasting no more than about 20 seconds in duration. The vapor HF etching cycle carried out pursuant to block 116 in Fig. 1 produces, for example, structure 260 of Fig. 2F.

Please amend the second full paragraph appearing on page 9 as follows:

The allowable duration of vapor HF etching is dependent at least in part upon the thickness of polyimide layer 206 (other factors affecting allowable etching duration include process parameters such as set out in Table 2). The greater the duration of etching, the deeper the etch. For example, given the etching parameters of Table 2, a polyimide layer 206 thickness of about 5.4 or 11.7 micrometers (measured before the curing step of block 114 in Fig. 1 which slightly reduces this thickness) enables an etch depth of about 4000 or 8000 angstroms, respectively. More specifically, an initial ~~polyimide layer~~ polyimide layer 206 thickness of about 5.4 or 11.7 micrometers is sufficient to produce a mask 220 that can sustain vapor HF etching (as described in Table 2) for at least about 40 or 80 seconds, respectively. (Such 40 or 80-second etching intervals are achieved through repetitive etch operations of about 20 seconds in duration each pursuant to the foregoing discussion.) Based upon the etch rate of the operation in Table 2, 40 or 80 seconds of etching results in an etch depth of about 4000 or 8000 angstroms, respectively, into ~~oxide~~ silicon dioxide layer 204 (i.e., dimension "y" in Fig. 2F).

Please amend the paragraph bridging pages 9 and 10 as follows:

Referring again to Fig. 2F, structure 260 is next subjected to a cleaning step pursuant to block 118. This step entails the immersion of structure 260 in deionized water for about 10 minutes at room temperature. Next, ~~polyimide~~ etching mask 220 is removed pursuant to block 120 (Fig. 1) using any method known in the art. For example, this etching mask 220 may be removed by immersing structure 260 in QZ 3321 polyimide stripper for approximately 25 minutes at about 100°C. This stripper is available from CIBA-Geigy Corporation, P. O. Box 2005, 540 White Plains Road, Tarrytown, New York 10591. Removal of ~~polyimide~~ etching mask 220 results in structure 262 of Fig. 2G, which includes an etched silicon dioxide layer 204 disposed over silicon substrate 202. Referring to Fig. 1, this resulting structure is subjected to a cleaning operation pursuant to block 122. In accordance with this operation, structure 262 is immersed in deionized water for approximately 15 minutes at room temperature.

Please amend the first full paragraph appearing on page 10 as follows:

Fig. 3 is a flow chart containing steps of an alternative etching process carried out pursuant to the principles of the invention. The etching process of Fig. 3 is prospective; i.e., it has not yet been practiced. Individually, each step may be performed through the use of conventional process techniques and materials well known to those having ordinary skill in the art. The most significant difference between the processes of Figs. 1 and 3 is polyimide type; the process of Fig. 1 uses non-photosensitive polyimide while the process of Fig. 3 uses photosensitive polyimide. Accordingly, the process of Fig. 3 eliminates use of a photoresist layer over the polyimide (e.g., blocks ~~106-110~~ 106, 108 and 110 of Fig. 1). Like the process of Fig. 1, the process of Fig. 3 may be performed on any etchable material, as described above. Fig. 4A, for example, shows etchable material in the form of a silicon dioxide layer 404 which is disposed on the surface of a silicon substrate 402. These layers combine to form ~~assembly~~ structure 450. In the following description, ~~assemblies 450-460~~ structures 450, 452, 454, 456, 458 and 460 (Figs. 4A-4F) will be used to illustrate the process steps set out in Fig. 3.

Please amend the first full paragraph appearing on page 11 as follows:

After deposition, polyimide layer 406 is exposed through a standard lithographical mask, pursuant to block 308 in Fig. 3. Such exposure alters the molecular structure of layer 406 in selected areas pursuant to a pattern defined by the lithographical mask 403. This step is illustrated in Fig. 4C, which shows a portion of a lithographical mask 403 disposed above polyimide layer 406. As described above, mask 403 selectively controls exposure of an underlying photosensitive surface to ionizing radiation 408 (e.g., ultraviolet light or low-energy x-rays). A portion of radiation 408 is stopped by mask 403 while the remainder is allowed to pass through the mask and alter the underlying material pursuant to the pattern of the mask. In this case, radiation 408 is allowed to expose polyimide layer 406 at area 410. The radiation exposure dose may be determined empirically or set as recommended by the polyimide manufacturer.

Please amend the paragraph bridging pages 11 and 12 as follows:

After exposure, polyimide layer 406 is developed by any technique known to those having ordinary skill in the art pursuant to block 310 of Fig. 3. In general, exposed polyimide layer 406 may be immersed in a suitable solvent that dissolves only exposed portions of the polyimide layer. This process produces structure 456 of Fig. 4D. As Fig. 4D shows, a portion of polyimide layer 406 has been removed leaving a gap 415. Accordingly, polyimide layer 406 is patterned in accordance with mask 403. Polyimide layer 406 is next cured, pursuant to block 314 of Fig. 3 using any technique known in the art. As in the process of Fig. 1, polyimide layer 406 will undergo a slight reduction in thickness due to this curing step. Thereafter, polyimide layer 406 forms an etching mask 420 over silicon dioxide layer 404. ~~Mask~~ Etching mask 420, having a pattern derived from lithographical mask 403 (Fig. 4C), will facilitate vapor HF etching, as described below.

Please amend the second full paragraph appearing on page 12 as follows:

Like polyimide layer 206 of Figs. 2B-2E, the thickness of polyimide layer 406 of Figs. 4B-4D controls, at least in part, the allowable duration of vapor HF etching. For example, it is believed a thickness of polyimide layer 406 of about 5.4 or 11.7 micrometers (measured before the curing step of block 314 in Fig. 3) will produce ~~a~~ an etching mask 420 (pursuant to blocks ~~308-314 of Fig. 1)~~ 308, 310 and 314 of Fig. 3) that can sustain vapor HF etching (as described in Table 2) for at least about 40 or 80 seconds, respectively. Such duration (applied in intervals of up to 20 seconds each, as described above) will enable an etch depth of about 4000 or 8000 angstroms, respectively, into ~~oxide~~ silicon dioxide layer 404 (i.e., dimension "y" in Fig. 4E). This is based on the same analysis as described above with respect to polyimide layer 206.

Please amend the third full paragraph appearing on page 12 as follows:

Returning again to Fig. 3, structure 458 is next subject to cleaning pursuant to block 318. This step is carried out in accordance with block 118 of Fig. 1. Next, polyimide mask 420 created out of layer 406 is removed pursuant to block 320. This step is performed in accordance with block 120 of Fig. 1. Removal of ~~polyimide~~ etching mask 420 results in structure 460 of Fig. 4F, which includes an etched silicon dioxide layer 404 disposed over silicon substrate 402. Referring to Fig. 3, this resulting structure is subject to a cleaning pursuant to block 322 of Fig. 3. Again, this process is carried out in accordance with block 122 of Fig. 1.

Please amend the paragraph bridging pages 12 and 13 as follows:

Vapor HF etching does not have the problems of wet etching noted above and therefore provides a method for etching small features. However, attempts to use this process with conventional photoresist (e.g., material such as OiR 89710i, available from OCG Microelectronic Materials, Inc.) have proven unsatisfactory since vapor HF will normally penetrate through a conventional photoresist layer functioning as a mask. For example, Fig. 5 illustrates a patterned, conventional photoresist 500 prior to etching with vapor HF. As shown, photoresist 500

(approximately 1.45 micrometers thick) contains no deformations except for patterned holes 502. In contrast, Fig. ~~6 illustrates~~ illustrates a patterned photoresist 500 after vapor HF etching. Significantly, large, irregular holes 602 are created by the etching process rendering the photoresist useless as a mask.

Please amend the first full paragraph appearing on page 13 as follows:

In contrast to conventional photoresist, polyimide has demonstrated very good characteristics for blocking vapor HF during etching. For example, Figs. 7 and 8 illustrate a non-photosensitive polyimide mask 700 (approximately 3 micrometers thick) before and after vapor HF etching, respectively. As these figures show, there is essentially no change in the structure of the mask. This is in stark contrast to photoresist 500 in Figs. 5 and 6, which ~~was~~ were etched for approximately the same duration and at the same etchant strength as mask 700. Thus, in accordance with the invention and as shown in Figs. 2F and 4E, a polyimide layer can serve as an effective mask for the etching process disclosed herein.

Please amend the second full paragraph appearing on page 13 as follows:

The use of polyimide as a mask in combination with vapor HF etching enables the creation of very small features (i.e., having dimensions of less than 1.0 micrometers) with a high degree of uniformity (i.e., a standard error of 5% in oxide etch rate has recently been achieved using vapor HF etching; see ~~Y. Ma~~ Ma et al., "Vapor Phase SiO_2 Etching and Metallic Contamination Removal in an Integrated Cluster System," J. Vac. Sci. Technol., B 13(4), pp. 1460-1465 (Jul./Aug. 1995), which is hereby incorporated herein by reference in its entirety for all purposes).

Please amend the paragraph bridging pages 13 and 14 as follows:

One preferred use of the invention is for exposing micropoint emitters during the fabrication of a field emission device (FED). Figure 9A shows a ~~cross-sectional~~ cross-sectional view of an FED 900 during an intermediate fabrication step of producing the FED 900. Dunn

this state of the fabrication process, FED 900 includes a baseplate 910, which is typically fabricated from silicon; a dielectric layer 912, which is typically fabricated from SiO_2 and is disposed over baseplate 910; and a layer of polysilicon 914 disposed over dielectric layer 912. As shown, a conical micropoint emitter 916 extends out of baseplate 910, and dielectric layer 912 and polysilicon layer 914 cover micropoint emitter 916. As is well known, to complete fabrication of the FED 900, a significant portion of the dielectric layer 912 must be removed so as to expose the micropoint emitter 916. Those skilled in the art will appreciate that FED 900 may include many micropoint emitters such as micropoint emitter 916, as well as other structures which for convenience of exposition are not shown in Figure 9A. FEDs such as FED 900 are discussed in greater detail in, for example, U.S. Patent Nos. 5,302,238 and 5,229,331.

Please amend the first full paragraph appearing on page 14 as follows:

The next step in the fabrication of FED 900 is to perform chemical-mechanical-planarization (using known methods) on FED 900 so as to planarize FED 900 along the dashed line 918 shown in Figure 9A. The result of such planarization is shown in Figure 9B. As shown, following ~~planarization~~ planarization, polysilicon layer 914 covers most of dielectric layer 912, however, a portion of dielectric layer 912 over micropoint emitter 916 is exposed by the planarization. So the planarization effectively patterns the polysilicon layer 914 so as to expose selected portions of the dielectric layer 912. Following this planarization, portions of the dielectric layer 912 that cover and surround micropoint emitter 916 are preferably removed so as to expose the micropoint emitter 916. Figure 9C shows the desired completed structure for FED 900 where an aperture 920 has been formed in dielectric layer 912 so as to expose micropoint emitter 916. However, prior art -processes for forming aperture 920, and thereby exposing micropoint emitter 916, have not performed adequately.

Please amend the paragraph bridging pages 14 and 15 as follows:

Part of the difficulty in forming aperture 920 is that the dimensions of the aperture 920 are not suitable for use with conventional wet etching processes. For example, the dimension of

the aperture ~~920~~ 920, proximal the upper surface of polysilicon layer 914, this dimension being denoted as "x" in Figure 9C, is relatively small (e.g., 0.3-0.7 μm). Further, the distance between the bottom of the aperture 920 (at the top surface of baseplate 910) and the top of the aperture 920, this dimension being denoted as "y" in Figure 9C, is relatively large (e.g., 0.8-1.0 μm), and the distance between the side of micropoint emitter 916 and the side of polysilicon layer 914 measured in a direction substantially perpendicular to these sides, this distance being denoted as "z" in Figure 9C, is also relatively small (e.g., 0.3-0.4 μm). These dimensions make conventional wet etching processes unsuitable for etching dielectric layer 912. As an example, air bubbles of a size comparable to the dimension "x", which typically form during wet etching can prevent the etching material from penetrating into the dielectric layer 912. Further, plasma etching is unsuitable for forming aperture 920 because such etching is likely to also etch the surface of micropoint emitter 916 and thereby dull or damage the relatively sharp tip of micropoint emitter 916. However, the vapor HF process described above may be applied to FED 900 to form aperture 920 by removing selected portions of the dielectric layer 912. The vapor HF process according to the invention is well suited for forming apertures of such dimensions as aperture 920.

Please amend the paragraph bridging pages 15 and 16 as follows:

The polysilicon layer 914 behaves in a similar fashion as the polyimide layers discussed above (e.g., polyimide layer 206 of Figures 2B-2D), and is resistant to the vapor HF etching process. So, a patterned polyimide protecting layer need not be formed over polysilicon layer 914 prior to initiating the vapor HF etching process according to the invention. In fact, rather than using polysilicon, layer 914 is a covering layer and may be implemented using a conductive, etch resistant material such as metal, silicon based materials, or other semiconductive materials. (Covering layer 914 functions in the FED as an extraction grid for drawing electrons from the micropoint ~~emitters).~~ emitters 916.) In the following description, polysilicon layer 914 will be discussed as being implemented with polysilicon, however, those skilled in the art will appreciate that other conductive, etch resistant materials could be ~~used.~~

~~Despite~~ used. Despite the etch resistance of polysilicon layer 914, it may be desirable to dispose ~~such~~ a polyimide layer over polysilicon layer 914 prior to initiating the vapor HF etching process. Figure 9D shows such a patterned polyimide layer 930 formed over polysilicon layer 914. Polyimide layer 930 is preferably formed after planarization of FED 900 as shown in Figure 9B. It is particularly desirable to form such a polyimide layer 930 over portions of the FED 900 which may not be covered (and thereby protected) by polysilicon layer 914.

Please amend the first full paragraph appearing on page 16 as follows:

In yet another variation, prior to forming a patterned polyimide layer 930 over polysilicon layer 914, a dielectric passivation layer may be formed over polysilicon layer 914 prior to formation of patterned polyimide layer 930. Such a dielectric passivation layer 932 is shown in Figure 9E. Passivation layer 932 is useful because it facilitates removal of polyimide layer 930. If passivation layer 932 is not used, and polyimide layer 930 is formed directly on polysilicon layer 914, the ~~layers~~ polyimide layer 930 and the polysilicon layer 914 may bond making the clean removal of polyimide layer 930 difficult. However, following formation of aperture 920 (shown in Figure 9C) polyimide layer 930 may be easily removed from passivation layer 932 using conventional techniques, and similarly, passivation layer 932 may be easily removed from polysilicon layer 914 also using conventional techniques.

Please amend the second full paragraph appearing on page 16 as follows:

When passivation layer 932 is used, the portion of passivation layer 932 over micropoint emitter 916 may be etched using the vapor HF etching process that is also used to form aperture 920 (shown in Figure 9C), or alternatively, this portion of the passivation layer 932 may be removed using dry or wet etching processes.